Thermal effects in Ni/Au and Mo/Au gate metallization AlGaN/GaN HEMT's reliability

M. F. Romero[1,2], M. J. Uren[3], A. Jiménez[4], C. Dua[5], M. J. Tadjer[1], *Member, IEEE*, R. Cuerdo[1], F. Calle[1] and E. Muñoz[1], *Member, IEEE*

(1) ISOM and Dep. Ing. Electrónica, ETSI Telecomunicación, Universidad Politécnica de Madrid, Spain.

(2) Institut für Experimentelle Physik, Otto-von-Guericke-Universität Magdeburg, Germany.

(3) QinetiQ, Malvern Technology Centre, Malvern, Worcestershire, WR14 3PS, United Kingdom.

(4) Dep. Electrón. Escuela Politécnica. Universidad de Alcalá, 28805 Alcalá de Henares, Madrid, Spain.

(5) III-V Lab, route de Nozay, 91461 Marcoussis Cedex, France.

AlGaN/GaN high electron mobility transistors (HEMT) are key devices for the next generation of high-power, high-frequency and high-temperature electronics applications. Although significant progress has been recently achieved [1], stability and reliability are still some of the main issues under investigation, particularly at high temperatures [2-3]. Taking into account that the gate contact metallization is one of the weakest points in AlGaN/GaN HEMTs, the reliability of Ni, Mo, Pt and refractory metal gates is crucial [4-6]. This work has been focused on the thermal stress and reliability assessment of AlGaN/GaN HEMTs.

After an unbiased storage at 350 ^{o}C for 2000 hours, devices with Ni/Au gates exhibited detrimental I_{DS}-V_{DS} degradation in pulsed mode. In contrast, devices with Mo/Au gates showed no degradation after similar storage conditions. Further capacitance-voltage characterization as a function of temperature and frequency revealed two distinct trap-related effects in both kinds of devices.

At low frequency (< 1MHz), increased capacitance near the threshold voltage was present at high temperatures and more pronounced for the Ni/Au gate HEMT and as the frequency is lower. Such an anomalous "bump" has been previously related to H-related surface polar charges [7]. This anomalous behavior in the C-V characteristics was also observed in Mo/Au gate HEMTs after 1000 h at a calculated channel temperatures of around from 250 ^{o}C (T2) up to 320 ºC (T4), under a DC bias (V_{DS}= 25 V, I_{DS}= 420 mA/mm) (DC-life test). The devices showed a higher "bump" as the channel temperature is higher (Fig. 1). At 1 MHz, the higher C-V curve slope of the Ni/Au gated HEMTs indicated higher trap density than Mo/Au metallization (Fig. 2).

These results highlight that temperature is an acceleration factor in the device degradation, in good agreement with [3]. Interface state density analysis is being performed in order to estimate the trap density and activation energy.

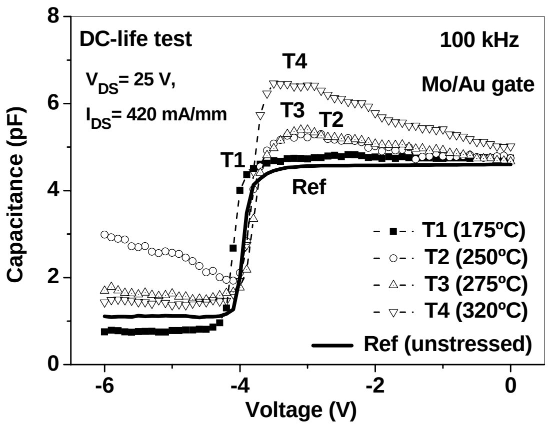


Fig. 1: Gate drain/source C-V characteristics at 100 kHz of AlGaN/GaN HEMT after DC-life test (1000 h) using Mo/Au gate metal.

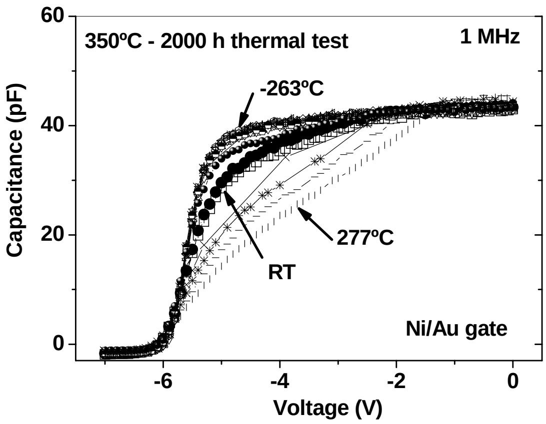


Fig. 2: Gate drain/source C-V-T characteristics at 1 MHz of AlGaN/GaN FAT FET after thermal storage at 350 ºC (2000 h) using Ni/Au gate metal.

References:

[1] M. Higashiwaki et al. Appl. Phys. Express, vol. 1, pp. 021103-1, -3, 2008.

[2] F. Danesin et al. Microelectr. Reliability, vol. 48, pp. 1361-1365, 2008.

[3] N. Malbert et al. IEEE International Reliability Physics Symposium (IRPS), pp. 139 – 145, 2010.

[4] J. Song et al. IEEE International Semiconductor Device Research Symposium 2005, pp. 254- 255.

[5] C. Lee et al. Electron. Letters, vol. 40, no. 24, pp. 1547-1548, 2004.

[6] A. Sozza et al. Electron. Letters, vol. 41, No. 16, 2005.

[7] Y. Irokawa. Sensors, Vol. 11, pp. 674-695, 2011.

Thermal effects in Ni/Au and Mo/Au gate metallization AlGaN/GaN HEMT's reliability

M. F. Romero[1,2], M. J. Uren[3], A. Jiménez[4], C. Dua[5], M. J. Tadjer[1], R. Cuerdo[1], F. Calle[1] and E. Muñoz[1]

[1]ISOM, ETSI Telecomunicación, Universidad Politécnica de Madrid, 28040, Madrid, Spain.
[2]Institut für Experimentelle Physik, Otto-von-Guericke-Universität Magdeburg, Germany.
[3]QinetiQ, Malvern Technology Centre, Malvern, Worcestershire, WR14 3PS, United Kingdom.
[4]Dpto. Electrónica, Escuela Politécnica Superior, Universidad de Alcalá, 28805, Alcalá de Henares, Madrid, Spain.
[5]III-V Lab, route de Nozay, 91461 Marcoussis Cedex, France.

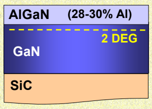
MOTIVATION & OBJECTIVES

- AlGaN/GaN high electron mobility transistors (HEMTs) are key devices for next generation of high-power, -frequency and -temperature electronics.
- Stability and reliability are still some of the main issues under investigation, particularly at high temperature.
- Gate contact metallization is one of the weakest points in AlGaN/GaN HEMTs, hence the reliability of metal gates is crucial.

→ This work focuses on the thermal stress and reliability assessment of AlGaN/GaN HEMTs with Ni/Au or Mo/Au gate metallization.

1 EXPERIMENTAL

- HEMT structure:



- Devices:
  - HEMT (L_G= 1.3 µm and L_G= 0.25 µm)
  - FAT-FET (L_G= 100 µm)
  - Gate contact: Ni/Au or Mo/Au

- Degradation tests:

⇒ Thermal storage: (unbias)

Cycle	Duration	Temperature
Short	14 hours	From RT to 300ºC (50ºC step + 30 min hold)
Medium	650 hours	300ºC
Long	2000 hours	250ºC
		300ºC
		350ºC

⇒ DC-life test: (bias) (only Mo/Au gate HEMTs, L_G= 0.25 µm)

Bias	Duration	Temperature	Calculated Channel Temperature*
V_{DS} = 25 V, I_{DS} = 420 mA/mm	1000 hours	10ºC	175ºC
		57ºC	250ºC
		71ºC	275ºC
		85ºC	320ºC

* Estimated from physical simulations and 3D thermal modeling.

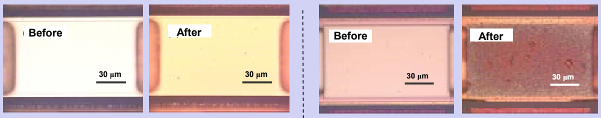
2 THERMAL STORAGE

➡ Thermal storage at ≤ 300ºC (≤ 2000 hours)

Both, Ni/Au and Mo/Au gate devices show
→ Increased Schottky barrier height (Φ_b)
→ High reduction up to 3 orders in reverse leakage current (I_{rev})

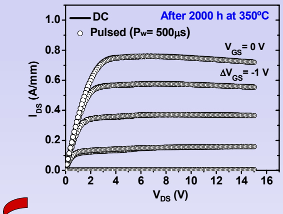
⇒ Enhanced both Ni/Au & Mo/Au gate contact induced by the soft thermal annealing

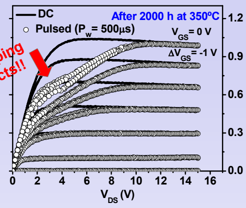
➡ Thermal storage at 350ºC (2000 hours)



Mo/Au gate　　Ni/Au gate

I-V (HEMT)



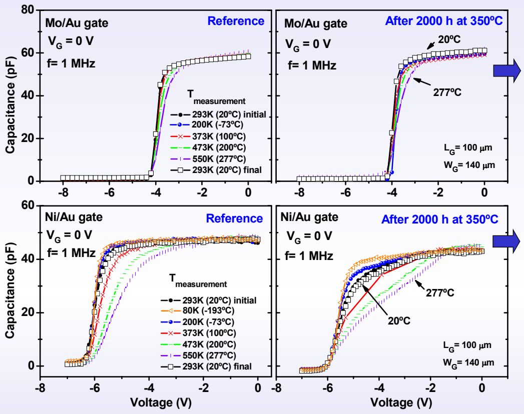


Mo/Au gate HEMT devices are more robust at 350ºC for 2000 h than using Ni/Au

At V_{DS}>> ➡ No trapping effects in Ni/Au
→ Different mechanisms became dominant

C-V-T (FAT-FET) ➡ Measured at low and high T in vacuum

High frequency (f = 1 MHz)

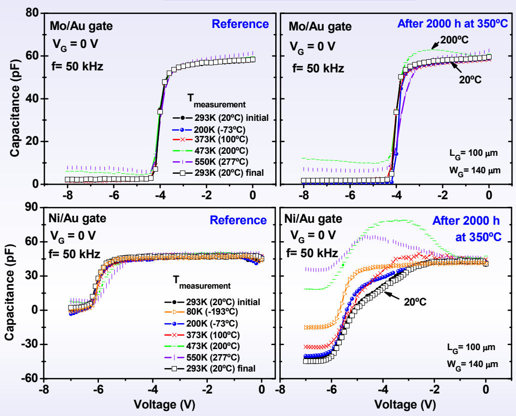


No significant changes in Mo/Au gate devices after long thermal storage at 350 ºC

Strong degradation increases with $T_{measurement}$ in Ni/Au gate devices after long thermal storage at 350 ºC

High occupancy of interface states was estimated using a modified Terman method [1]: (D_{it} ~ 10^{14} $cm^{-2}\cdot eV^{-1}$ near the conduction band at RT)

Low frequency (f = 50 kHz)



Slight presence of slow traps in Mo/Au gate devices after long thermal storage test at 350ºC

Strong C-V dispersion in Ni/Au gate devices, in particular for $T_{measurement}$ > -100ºC and f< 350 kHz, after long thermal storage at 350ºC

Assuming the rise in C is related to presence of traps beneath the gate and one single energy level approximation [2], the trap response time and energy are estimated

τ = 62 µs

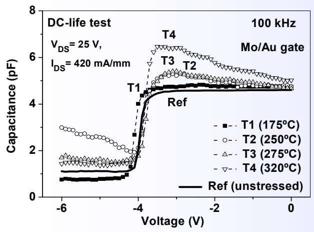
E_T= 340 meV → Could be related to donor defects [3]

Capacitance characteristics in FAT-FET devices correlate the results in HEMTs showing higher thermal stability in Mo/Au gate devices, even at 350ºC for 2000 hours, in contrast to those using Ni/Au gates.

These results are in good agreement with Sozza *et al* that showed no metal diffusion in AlGaN after a similar long themal storage test [4].

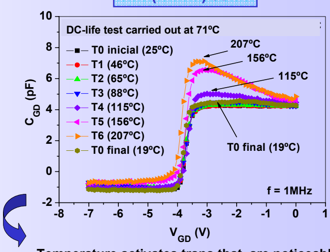
3 DC – LIFE TEST

C-V (HEMT) at RT



Mo/Au gate HEMTs shows anomalous C-V behaviour after DC life tests carried out at T > 10ºC ($T_{channel}$> 175ºC)

C-V (HEMT) at HT



Temperature activates traps that are noticeable at high frequency (1 MHz) for higher $T_{measurement}$ than at lower frequencies.

Estimated energy (E_T= 2.2 eV)

Although Mo/Au scheme leads to high thermally stable gate devices, noticeable degradation is still observed after electrical stress probably due to AlGaN surface traps.

These results are in good agreement with Malbert *et al* that showed a degradation in Mo/Au HEMTs after a similar DC-life test likely due to surface defects under the gate [5].

CONCLUSIONS

- Gate contacts of Ni/Au and Mo/Au improves after soft baking (up to 300ºC), reducing leakage current.
- Mo/Au gate devices turned to be thermally more stable than Ni/Au gate devices, in particular at 350ºC for 2000 hours.
- However, Mo/Au gate HEMTs degrade after harsh bias stress showing an increase of trapping effects.

REFERENCES

[1] D. Deen *et al*. Appl. Phys. Lett., vol. 98, pp. 023506, (2011).
[2] D. K. Schroder, 3ª Ed, 2006.
[3] T. Hashizume *et al*. Appl. Surf. Scien., vol. 234, pp. 387-394, (2004).
[4] A. Sozza *et al*. Electron. Letters, vol. 41, no. 16, pp. 927-928, (2005).
[5] N. Malbert *et al*. IEEE International Reliability Physics Symposium (IRPS), pp. 139 – 145, (2010).

ACKNOWLEDGMENT

This work was supported by RUE project (CSD2009-00046) and AEGAN (TEC2009-14307-C02-01) projects from Ministerio de Ciencia e Innovación of Spain, and in part by the KORRIGAN project (EDA—04/102.052/032 CA 2157v7). F.T. acknowledges the financial support by the EU within the 7th RTD Framework (project RAINBOW: Contract No. PITN-GA-2008-213238).